TITLE OF THE INVENTION

PROCESS AND CIRCUIT ARRANGEMENT FOR DIGITAL FREQUENCY CORRECTION OF A SIGNAL

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of and priority to International Application PCT/DE00/03601, filed October 11, and German Patent Application GR 99 P 5026, filed October 11, 1999, the contents of each of which are incorporated herein.

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0002] The invention relates to a process and a circuit arrangement for digital frequency correction of a signal, in particular for use in a transceiver circuit, [according to the preamble of claim 1 or 7] by sampling the signal with a predetermined cycle and processed using an N-step CORDIC algorithm so that a frequency of the signal is altered by a predetermined frequency.

2. Description of the Related Art

[0003] In transceiver circuits, local oscillators are used [for producing] to produce a reference frequency. Particularly because of production tolerances, temperature fluctuations, and supply voltage fluctuations, undesired fluctuations of the reference frequency can occur. [This] The undersigned fluctuations of the reference frequency causes [the] a signal to be processed [likewise to have] having large frequency fluctuations, and [the] a power of the transceiver circuit is thereby reduced.

[0004] In order to counteract [this] the undesired fluctuations, expensive and high quality oscillators are, for example, used in the transceiver circuits, [and] to produce a very stable reference frequency, i.e., [one] an oscillator which is precise and free from fluctuation. Likewise, oscillators compensated for voltage fluctuations and for temperature variations can also be used to reduce [the] a dependence [of] on the reference frequency [on] for the voltage fluctuations and the temperature variations. Furthermore, so-called automatic frequency correction control loops (AFC loops) are frequently used [for] to precisely [setting] set the local reference frequency. However, [it is] the AFC loops are disadvantageous in that [these solutions are on the one hand] the AFC loops are expensive and [on the other hand] very costly in circuit

technology.

[0005] In order to keep the costs of [a] the transceiver low, in particular for use in mass produced articles, such as mobile telephones, [the use presents itself of] cheap oscillators have been used which have neither a voltage supply control device nor a temperature control device. However, particularly in such products, no excessive fluctuation of the reference frequency can be tolerated. A subsequent correction of the frequency of the signal[s] to be processed is therefore unconditionally necessary.

[0006] A frequency correction process of a baseband signal x in a transceiver circuit, for example of a mobile radio receiver, can be represented mathematically as follows: [The] sampling values x(k) of the baseband signal x(k) = i(k) + j q(k) (with j = sqrt(-1)), [the] symbols [of] which have a symbol duration T, are multiplied by [the] sampling values of a (complex) frequency correction signal z(k) = $2\pi t$ T/m k, m being [the so-called] an oversampling factor[; this]. The multiplication in [the] a time domain corresponds in [the] a frequency domain to a frequency displacement of the baseband signal x(k) by [the] a frequency f. In [the] a complex signal pointer plane, [this] the multiplication represents a rotation of the "pointer" x(k) through [the] an angle z(k):

$$x(k)\ \exp(j\ z(k)) = [i(k) + j\ q(k)][\cos(z(k)) + j\ \sin(z(k))]$$
$$= [i(k)\cos(z(k)) - q(k)\sin(z(k))] + j\ [i(k)\ \sin(z(k)) + q(k)\ \cos(z(k))]$$

[0007] The more precise[ly] and more finely adjustable [the] a frequency correction signal z(k), the better the frequency correction [is effected]; i.e., the "pointer" x(k) can be rotated in finer steps in the complex plane.

[0008] [It would for example to calculate the] The frequency correction according to the above equation may be calculated using [by means of] digital multipliers and coefficient tables for [the] a sine and cosine functions; [this] which demands, though, a very high circuit technology cost which makes such a solution expensive and costly. In particular, when embodied as an integrated circuit, this solution requires a large chip surface and is, therefore, very expensive.

SUMMARY OF THE INVENTION

[0009] The invention therefore has as its object to provide a process and a circuit arrangement for digital frequency correction, particularly for use in a transceiver circuit, which produces a very precise frequency correction with a small circuit technology cost.

[0010] [This] The above and other objects [is] are attained [by means of] using a process [with the features of claim 1 and a device with the features of claim 7. Developments of the invention will become apparent from the dependent claims].

[0011] [A fundamental concept of the invention is to use the] An exemplary embodiment of the present invention includes an CORDIC (Coordinate Rotation Digital Computer) algorithm for [the] digital frequency correction of a signal. Namely, a frequency and phase correction can be carried out relatively simply [by means of] using the CORDIC algorithm[, and the]. The CORDIC algorithm can be carried out with a small circuit technical cost, so that [the] costs of a circuit based on [it -- cheaper oscillator and CORDIC correction --] the CORDIC algorithm and an inexpensive ocillator are smaller than [with a costly] the costs of a compensated oscillator.

[0012] The CORDIC algorithm is described in J.E. Volder, "The CORDIC trigonometric computing technique", IRE Trans. Electronic Computers, Vol.8, pp. 340-344, 1959[; the]. This algorithm is n-fold iterative and serves to rotate a vector through a defined angle $\alpha_n = \arctan(2^{-n})$, n = 0, 1, ..., N-1. If the vector represents[, as described at the beginning, the] a pointer of a complex signal, [the] a change [of the] in a frequency of the signal corresponding to a multiplication by a frequency correction signal is possible by means of this rotation. The rotation angle becomes smaller with each iteration ($\alpha_0 = 45° > \alpha_1 = 26.6° > \ldots > \alpha_{N-1}$, so that the frequency of the signal changes in [smaller and] smaller steps with increasing iteration steps.

[0013] The iterative rotation through an angle a can be represented by the following linear combination:

$$a = \sigma_0\alpha_0 + \sigma_1\alpha_1 + \ldots + \sigma_{N-1}\alpha_{N-1} \qquad (\sigma_n = \pm 1)$$

[0014] [The] A precision of the rotation is predetermined by the smallest rotation angle α_{N-1}. [The] A direction of rotation (+1 counterclockwise, -1 clockwise) is given by the sign σ_n.

[0015] A signal which is represented by sampling values of the in-phase component I_n and

the quadrature component Q_n is [now] iteratively rotated through the angle a by [means of] the CORDIC algorithm. For this purpose, the individual rotations according to the CORDIC algorithm can be executed by simple shift and addition operations:

$$I_{n+1} = I_n - \sigma_n 2^{-n} Q_n$$

$$Q_{n+1} = \sigma_n 2^{-n} I_n + Q_n$$

[0016] The above equation can also be represented as follows, using the equation $\alpha_n = \arctan(2^{-n})$ for the rotation angle:

$$I_{n+1} = \mathrm{sqrt}(1 + 2^{-2n}) \, [\cos(\sigma_n \alpha_n) \, I_n - \sin(\sigma_n \alpha_n) \, Q_n]$$

$$Q_{n+1} = \mathrm{sqrt}(1 + 2^{-2n}) \, [\sin(\sigma_n \alpha_n) \, I_n + \cos(\sigma_n \alpha_n) \, Q_n]$$

[0017] After N rotations, [there] the following is obtained:

$$I_N = K \, [\cos(z) \, I_0 - \sin(z) \, Q_0]$$

$$Q_N = K \, [\sin(z) \, I_0 + \cos(z) \, Q_0]$$

with K = 1.647. The signal to be corrected can be adjusted in frequency [by this means] using the process described above.

[0018] In the process according to the invention, the complex multiplication of the sample values x(k) of [a] the signal, particularly of a baseband signal, by [a] the frequency correction signal z(k) is now executed [by means of] using the CORDIC algorithm. [Since there takes place in] Because a principle no "rigid" frequency correction occurs, [but] and a frequency correction which is variable because of the CORDIC algorithm, the constancy of [the] a reference signal of [an] the oscillator does not play a [large] significant part.

[0019] In order to use the CORDIC algorithm for the process according to the present invention, a few disadvantages of the CORDIC algorithm must however be compensated for by the invention[:]. In particular, because [Since] the CORDIC algorithm [makes possible] allows only a limited correction range of a rotation angle of approximately 99°, a reduction of the rotation angle required for correction is required. It is provided, according to the invention, for this purpose to correct the rotation angle so that [it] the rotation angle always has a value less

than or equal to 90°. The rotation angle represented by z(k) is a stored modulo 2π in a register of a bit width N_w. The value w(k) stored in the register is accumulated according to [the] an equation $w(k) = w(k-1) + f \cdot T/m$. [The] A value 111...111 for w(k) corresponds to [the] a greatest value $1 - 2^{N}_{w}$, corresponding to an angle of $2\pi\ (1 - 2^{N}_{w})$[; the]. The modulo 2π operation is, thus, attained by simply neglecting [the] an overflow of the register.

[0020] Furthermore, [it is required for] in order to provide optimum execution of the CORDIC algorithm, [that] the pointer z(k) needs to be represented by [the] a frequency correction signal [lies] lying in [the] a first or a fourth quadrant of [the] a complex I/Q plane. For this purpose, [it is provided that the] an in-phase and quadrature components of the pointer of the signal to be corrected are respectively multiplied by $(-1)^s$, s = 0.1, in order [then] to turn the pointer through the angle $z(k) - \pi$ when the pointer lies in [the] a second or a third quadrant of the complex I/Q plane.

[0021] [The] A sign flag s is calculated like the sign σ_n for the individual iterations (micro-rotations) of the CORDIC algorithm. According to the invention, a sign table is provided for this purpose, in which the corresponding sign of the micro-rotation is set out for all possible micro-rotations, such that the sign flag s and the two signs σ_0 and σ_1 are calculated directly and the remaining signs σ_n, n = 2, 3, ..., N-1 are calculated from the bits w_1, w_2, w_3, ..., w_{N+1} of [the] a value w(k) stored in the register.

[0022] The bit width N_w of the register and the number of micro-rotations N of the CORDIC algorithm affect the correction range or [the] a phase noise of the frequency-corrected signal $x(k) \exp(jz(k))$ and are therefore to be chosen according to the present invention as follows. [The] A bit width N_w is to fulfill the following inequality for a correctable frequency range Δf:

$$N_w \geq \log2(m) - \log2(\Delta f \cdot T)$$

[0023] For a desired signal to phase noise ratio SNR, [the] a number N of the micro-rotations is chosen as follows:

$$(SNR + 3)/6 \leq N \leq N_w - 2$$

[0024] The desired signal to phase noise ratio SNR is thus attained, [the] an upper limit for N being predetermined by the bit width of the register.

[0025] Finally, another two guard bits have to be provided in each iteration of the algorithm during the implementation of the CORDIC algorithm, in order to be able to process the greatest possible value of the scaling factor, namely sqrt(2) K = sqrt(2) 1.647 2.33. K is [the] a scaling factor because of the CORDIC algorithm and sqrt(2) is [the] a possible "growth factor" of the in-phase and quadrature components due to the CORDIC algorithm. Accordingly, [the] an input bit width and an output bit width of the CORDIC algorithm should be as great as possible, [preferably] for instance, at least greater than N + 2. A greater phase noise would otherwise be produced by rounding errors of the CORDIC algorithm than by phase errors.

[0026] These together with other objects and advantages, which will be subsequently apparent, reside in the details of construction and operation as more fully hereinafter described and claimed, reference being had to the accompanying drawings forming a part hereof, wherein like numerals refer to like parts throughout.

BRIEF DESCRIPTION OF THE DRAWINGS

[0027] The following description of preferred embodiments of the invention, using the accompanying drawings, serves for further explanation of the invention.

[Fig.] FIG. 1 shows a block circuit diagram with [the] essential components for carrying out [the] a process according to the invention,

[Fig.] FIG. 2 shows [the] a structure of a sign table for [the] a CORDIC algorithm,

[Fig.] FIG. 3 shows [the] a structure of a micro-rotation block for [the] a CORDIC algorithm, and

[Fig.] FIG. 4 shows [the] a use of the process, according to the invention, in a transceiver of a GSM mobile telephone.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0028] In [Fig.] FIG. 1, sampling values i_0 and q_0 of [the] an in-phase or quadrature components of a complex baseband signal x(k) are supplied to a quadrant correction block 10, where [(]k denotes [here the] discrete sampling times[)]. The quadrant correction block 10 causes [the] a pointer represented by the baseband signal x(k) to lie in [the] a first or fourth quadrant of [the] a complex in-phase/quadrature I/Q plane. Namely, if the pointer lies in [the] a second or third quadrant, [the] CORDIC algorithm does not work correctly. As already

described, the in-phase and quadrature components have to be respectively multiplied by -1 if the pointer is situated in the second or third quadrant of the complex I/Q plane.

[0029] N micro-rotation blocks in sequence follow the quadrant correction block 10[;] although [only] three of these blocks, 11, 12, 13, are shown, a one of ordinary will appreciate that more blocks may be implemented. Each micro-rotation block calculates a step of the CORDIC algorithm, i.e., rotates the pointer represented by the in-phase and quadrature components in the complex I/Q plane through an angle $\pm \alpha_n = \pm \arctan(2^{-n})$. [The components] Components I_0 and Q_0 are present at [the] an input of [the] a micro-rotation block 11, and represent at [the] an output, as the components I_1 and Q_1, a pointer rotated through the angle $\pm \alpha_0 = \pm \arctan(1)$. The components I_2 and Q_2 are present at [the] an output of [the] a micro-rotation block 12, and represent a pointer rotated through an angle $\pm \alpha_1 = \pm \arctan((2^{-1}))$. Finally, a pointer represented by [the] in-phase component[s] I_n and an original quadrature Q_n and representing the frequency-corrected complex baseband signal is present at [the] an output of [the] a micro-rotation block 13 after passage through N steps of the CORDIC algorithm. The rotation is either counterclockwise or clockwise in each rotation in a micro-rotation block. The direction of rotation depends on [the] a sign σ_n.

[0030] The sign σ_n and [the] an input signal s for the quadrant correction block 10 are produced by [the] a sign table 14. The sign table 14 is driven by a register 31 with a bit width N_w in which a register value w with N_w bits is deposited. The first (N+2) bits of w(k) of [the] a register 31 are supplied to the sign table 14.

[0031] The structure of the sign table 14 is shown in [Fig.] FIG. 2. The input signal s for the quadrant block 10 is calculated by a logical XOR operation 16 on [the] two lowest bits w_0 and w_1 of the register value w. [The] A first sign σ_0 corresponds directly to the bit w_1 of the register value w. [The] A second sign σ_1 is calculated by inverting 17 [the] a bit w_2 of the register value w. [The remaining] Remaining signs σ_2 through σ_{N-1} are deposited in a read-only memory 15 (ROM), in which 2^N (N-2) bits are stored. The ROM or read-only memory 15 can be made smaller by [the] a calculation of s, σ_0 and σ_1 from the three lowest bits w_0-w_2; namely, a memory capacity of 2^{N+2} (N + 1) bits would otherwise be required.

[0032] The following table clarifies the calculation of s, σ_0 and σ_1 from the three lowest bits w_0 through w_2 of the register value w, and [the] a corresponding rotation angle range:

w_0	w_1	w_2	Rotation angle range		Quadrant	s	σ_0	σ_1
0	0	0	0°	45°	I	0	0	1
0	0	1	45°	90°	I	0	0	0
0	1	0	90°	135°	II	1	1	1
0	1	1	135°	180°	II	1	1	0
1	0	0	180°	225°	III	1	0	1
1	0	1	225°	270°	III	1	0	0
1	1	0	270°	315°	IV	0	1	1
1	1	1	315°	360°	IV	0	1	0

[0033] The signs σ_n are coded such that a logical "0" means a counter-clockwise rotation and a logical "1" means a clockwise rotation. [The input] Input bits of the sign table 14, i.e., of the register value w, are calculated cumulatively, w(k) = w(k-1) + f•T/m, starting from the default value f•T/m. An adder 18 and a delay element 19 are provided for this purpose. The delay element [18] 19 delays the last register value w(k-1) by the time T/m. The adder 18 then adds the default value f•T/m, which predetermines [the] a correction frequency f, to w(k-1). [The] A result of the addition then gives [the] a new register value for the register 31.

[0034] The structure of a micro-rotation block, which calculates the basic CORDIC operation previously described [at the beginning],

$$I_{n+1} = I_n - \sigma_n 2^{-n} Q_n$$

$$Q_{n+1} = \sigma_n 2^{-n} I_n + Q_n$$

is shown in [Fig.] FIG. 3. For this purpose, a first and a second shift register, 20 or 21 respectively, are provided, respectively shifting the in-phase component I_n or the original quadrature component Q_n by n bits (2^{-n}). The in-phase component or the original quadrature component shifted by n bits is then multiplied by the sign σ_n or $-\sigma_n$, i.e., the sign of the displaced component is correspondingly altered, and is added to the original quadrature component Q_n or

in-phase component I_n in a first 22 or second 23 accumulator, respectively. The result is a rotated pointer, represented by the in-phase component I_{n+1} and the quadrature component Q_{n+1}.

[0035] [Fig.] FIG. 4 shows [the preferred] an exemplary use of the process according to the present invention in a transceiver of a GSM mobile telephone. Sampling values x(k) of a baseband signal are supplied to a digital prefilter 24 which is operated with a high cycle rate, which is a multiple of [the] a sampling rate of 2 of the baseband signal.

[0036] Following the digital prefilter 24 is a first decimator 25, which divides the high cycle rate of the output signal of the prefilter 24 into a lower cycle rate. The first decimator 25 is provided with an offset compensation block 26 for the compensation of a DC offset, i.e., a DC portion, possibly contained in the baseband signal. The DC offset to be compensated is predetermined for the offset compensation block 26 by a digital signal processor 30. The digital signal processor 30, based on first sampling values of the baseband signal, estimates an offset or DC portion possibly contained in the baseband signal, and supplies [this] the estimated offset or DC portion to the offset compensation block 26 for compensation. If [an] the offset or the DC portion of the baseband signal [were not] is removed, [this] the offset would be transformed by the CORDIC algorithm into an interfering sine signal, which for example, is only to be expensively removed again in the digital signal processor 30.

[0037] The offset compensation block 26 is followed by a CORDIC frequency correction block 27 for carrying out the process according to the present invention. The correction frequency f by which the baseband signal is to be corrected is supplied to the CORDIC frequency correction block 27 by the digital signal processor 30. The CORDIC frequency correction block 27 corrects the baseband signal frequency, as previously described, by the correction frequency f.

[0038] The CORDIC frequency correction block 27 is followed by a digital postfilter 28, which is cycled at precisely twice the sampling rate 2 of the baseband signal. The digital postfilter 28 is a low pass filter with a [very great] large edge steepness and serves to remove interfering frequencies and noise of the baseband signal.

[0039] The frequency-corrected and [plurally] many times filtered baseband signal is then decimated by a second decimator 29 by [the] a factor 2 to the sampling rate of the baseband

signal, and is supplied to the digital signal processor 30 for further processing.

[0040] [It should be mentioned here that the] The process according to the present invention and the corresponding device for carrying out the process [are] may also [preferred for use] be used for frequency correction in [the] a transmitter and a receiver of a UMTS (Universal Mobile Telecommunication System) mobile radio device. A further application is [the] a use of the process according to the present invention everywhere in transmitters and receivers where the process according to the invention and the corresponding device serves, in addition to frequency correction, also for digital frequency mixing. [Since] Because the functions of frequency correction and frequency mixing are very often used, traditional mixers can be saved in this manner and thus the cost can again be markedly reduced. Examples of such a transmitter and receiver are found in cordless telephones of the DECT standard (Digital Enhanced Cordless Telephone), DVB (Digital Video Broadcasting), and cable modems.

[0041] Although the preferred embodiments of the present invention have been disclosed for illustrative purposes, those skilled in the art will appreciate that various modifications, additions and substitutions are possible, without departing from the scope and spirit of the invention as disclosed in the accompanying claims.